# A BATTERY-POWERED, SOLID-STATE MAGNETIC COMPRESSOR WITH APPLICATIONS FOR HIGH-PRF ACCELERATORS AND LASERS*

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## Abstract

An 8-J/pulse magnetic pulse compressor has been built to demonstrate a power conditioning technique whereby battery power is converted into a train of 5-μs pulses at a maximum pulse repetition frequency of 11 kHz. The machine employs inverter-grade thyristors that switch with less than 120-ps pulse-to-pulse jitter. The network uses a phased-triggering scheme to obtain an output voltage regulation of ±0.002%. Magnetic core reset is achieved by using a reflected portion of the output pulse from a mismatched load.

## Introduction

The baseline design for a proposed large-scale induction linear accelerator includes battery-powered, 1500-J/pulse thyristor-based pulse-power units. These units produce 15-μs-wide, 10-kHz pulses to drive magnetic pulse compressors. For proper linac operation the output pulses must be voltage-regulated to ±0.04% and have a timing jitter of less than 120 ps.[1]

Preliminary design work on the baseline pulse power units includes a subscale test model from which test results have confirmed that design goals can be achieved. The model, as originally conceived, was configured to accept a single silicon-controlled rectifier (SCR) as the switching element. A more recent version uses three SCRs in series as switches. The output is a voltage-regulated, 5-μs, half sinusoid, 8-kA, 10-kHz pulse train at either 600 V (single SCR) or 1800 V (three SCRs). Energy produced by the 600-V version is 8 J/pulse and by the 1800-V is 24 J/pulse.

The full-scale modulator will use a series-parallel array of SCRs to drive multiple compression stages, which, in turn, will charge a water-filled pulse-forming line (PFL). The PFL output is an 80-ns, 1500-J pulse that drives induction cells of a linear accelerator.

Figure 1 is a circuit schematic, while Table 1 gives a brief description of each stage of the test model. The following sections describe each circuit stage in more detail.

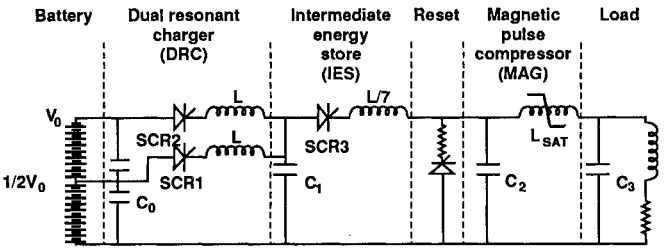


**Figure 1. Circuit schematic of test model.**

## Theory of Operation

### Dual Resonant Charger

The dual resonant charger (DRC) is a resonant circuit operated in the repeated transient mode. Since $C_0 >> C_1$, triggering SCR2 will cause the voltage on $C_1$ to resonate up to the theoretical value of $2V_0$. In practice, the value is somewhat less ($1.92V_0$) because of resistive losses in the inductor, capacitor, SCR, and SCR snubber.

The DRC shown in Fig. 2 has two resonant paths. If only SCR1 is triggered, the voltage $V_1$ on capacitor $C_1$ will resonate up to $V_0$. In operation, any voltage between $V_0$ and $2V_0$ can be realized by phasing the trigger delay between SCR1 and SCR2 (see Fig. 3).

Both feed-forward and feedback techniques are used. The feed-forward regulator monitors the battery filter-bank voltage and predicts the trigger phasing required to boost the input voltage to the desired output voltage.

The proper trigger phase vs input voltage characteristic can be obtained through analysis or measurement. Analytically (ignoring losses and source impedance), the characteristic waveform for a constant-voltage output is

**Table 1. Description of circuit schematic of Fig. 1.**

| Section (from Fig. 1) | Description |
|---|---|
| Battery (lead acid) | Primary power source consists of three 600-V, 3.2 A·H, center-tapped, 20-kW, 45-s each; choice of series or parallel configuration. |
| Dual Resonant Charger (DRC) | Resonantly charges $C_1$ to a predetermined voltage and isolates power supply after voltage recovery. |
| Intermediate Energy Store (IES) | Resonantly charges $C_2$ (MAG input) while providing a factor of ~4 switch compression (55 μs to 15 μs). |
| Reset circuit | The saturable inductor, $L_{sat}$, must be reset after each saturation event. The reset circuit, in conjunction with load mismatch, accomplishes this. |
| Magnetic pulse compressor (MAG) | Magnetically compresses the output pulse of the IES by a factor of 3 and delivers the 5-μs pulse to the load. |
| Load | The actual load is simulated with an appropriate LRC circuit. |

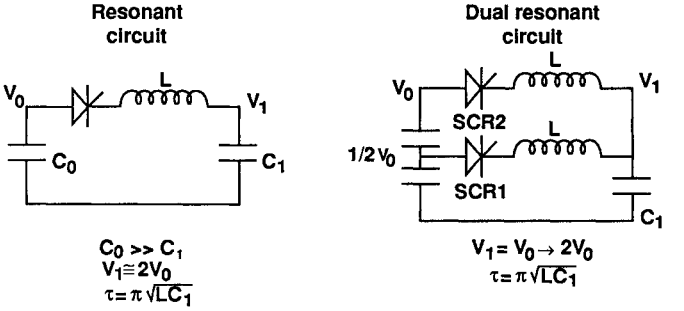


**Figure 2. Resonant circuit and dual resonant circuit.**

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14. ABSTRACT
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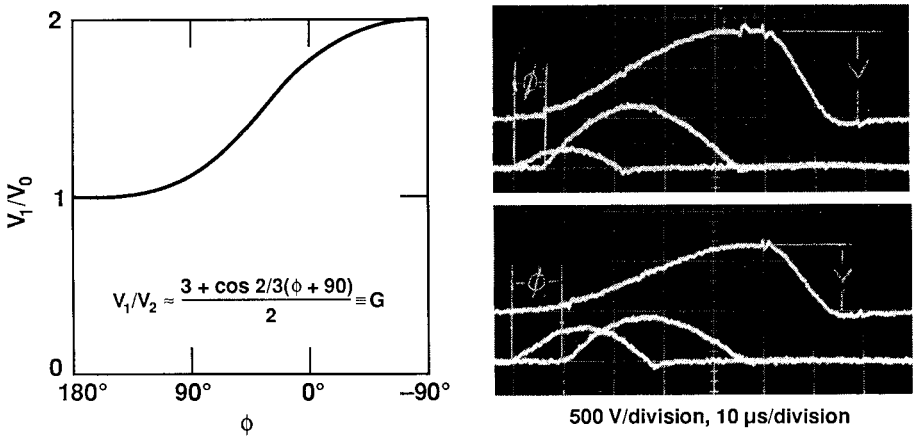


**Figure 3. Output voltage vs trigger phase of dual resonant circuit.**

simply the inverse of the transfer function, G, shown in Fig. 3. Once obtained, the characteristic waveform is placed in the memory of an arbitrary-function generator and output on channel 1 of the regulator circuit of Fig. 4. The waveform is time-correlated with the trigger phase of SCR2 and compared with the input voltage from the battery. The comparator then triggers SCR1 at the point on the characteristic waveform that will boost the input battery voltage to the proper output value.

The resulting regulator is:

- Tolerant of 50% input voltage variations (nominally caused by internal resistance drops in the batteries).
- Loss-minimizing (regulating adds no additional loss above normal conduction losses).
- Immune to self-generated noise and electromagnetic interference (measurement, comparison, and triggering are done with the pulse-power circuit quiescent).
- Robust (only naturally commutated high-power SCRs are used).

A dual-channel arbitrary-function generator with 5-ns-per-point waveform storage, when combined with an SCR exhibiting subnanosecond turn-on time jitter and a pure dc source (battery), has allowed short-term voltage regulation on capacitor $C_1$ of ±0.002% (Fig. 5).

The limitation of the feed-forward technique is that it is open loop. Temperature-induced effects, notably in capacitor values and inductor Q, cause long-term drifts that must be corrected to maintain voltage regulation at the desired precision. An outside feedback loop is invoked to make this correction. The feedback portion of the circuit of Fig. 4 obtains a correction signal by comparing the output voltage to a given reference, adding the amplified difference to the previous correction signal, and applying this new correction signal as a bias to the characteristic waveform. Since temperature-induced variations in the dielectric constant ($\varepsilon_r$) of the PFL rise to the largest variations in capacitance, the feedback signal will have to be sampled, held, and averaged at the pulse-line output or at an electron-beam-energy analyzer at the output of the accelerator.

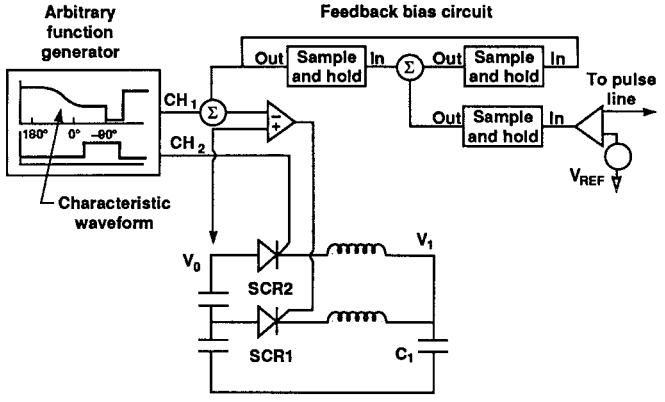


**Figure 4. Regulator circuit using dual resonant action.**

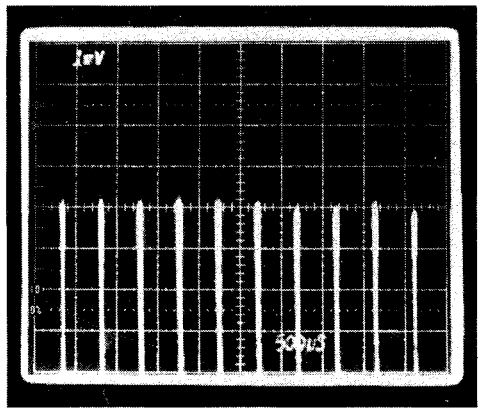


**Figure 5. Voltage regulation on capacitor $C_1$.**

## Intermediate Energy Store

The intermediate energy store (IES) resonantly transfers the energy in capacitor $C_1$ to $C_2$. This circuit is basically the same resonant circuit as that operating in the DRC but at a shorter pulse width. Also, since $C_1 = C_2$, then $V_1 = V_2$ and $\tau = \pi\sqrt{L\frac{C_1}{2}}$.

The pulse width chosen ($\tau$ = 15 μs) is a compromise between having a cost-effective, multimegawatt, solid-state switch (> $\tau$) and a magnetic pulse compressor with adequate reset and jitter (< $\tau$).

The active switching elements are crucial components in the pulse modulator. Also, the IES switch is stressed with high peak-power requirements. A correctly selected, properly applied switching device is vital to the success of the equipment.

Component testing at Lawrence Livermore National Laboratory determined that the Westcode R355A2W thyristor was an appropriate match to our requirements. A validated operating point is shown in the test results section.

## MAG Reset

$L_{sat}$, shown in Fig. 2, is a saturable magnetic core used as a magnetic switch. The high relative permeability of the metal-glass material (Metglas 2605CO) effectively isolates capacitor $C_2$ from $C_3$ when the IES is charging $C_2$.[2]

If the amount of volt-seconds designed into the core is selected properly, saturation will occur simultaneously with the completion of the charging of $C_2$. After saturation, $C_2$ will resonate into the load with a resonance time determined by $C_3$ and the saturated inductance of $L_{sat}$, i.e., 5 μs. Temporal compression of the 15-μs IES output pulse is realized in this manner.[3]

If the core is to be ready for the next pulse, which can come in as little as 90 μs, it must be reset by applying the same amount of volt-seconds in

reverse. Resetting is facilitated by the load characteristic of an induction accelerator, which causes a negative voltage reflection to appear on $C_2$ after one round-trip transit time of the MAG. This reflection (≅5% power, –30% voltage) resides on $C_2$ until $L_{sat}$ is reset (saturated in reverse). At this point the reflection would continue for another round trip if the reset circuit were not initiated. Reset is sensed by a rising di/dt in the saturable core, and at this point the remaining energy in $C_2$ is promptly switched out of the capacitor and dissipated in the reset circuit (see reset circuit initiation in Fig. 6). An important point to note is the 6-μs time interval between the discharge of the first MAG capacitor and the return of the reflected voltage. This 6 μs plus the 5 μs it takes the MAG capacitor to discharge is the time allowed for the IES SCRs to recover voltage-holding capabilities before the voltage reflection reapplies a forward bias. While the recovery times allowed by all other aspects of circuit operation can be controlled by pulse timing, this recovery time is fixed. Circuit testing has shown the recovery time with conditions supplied by the test stand circuit to be less than 10 μs, which is sufficient for the waveform shown in Fig. 6.

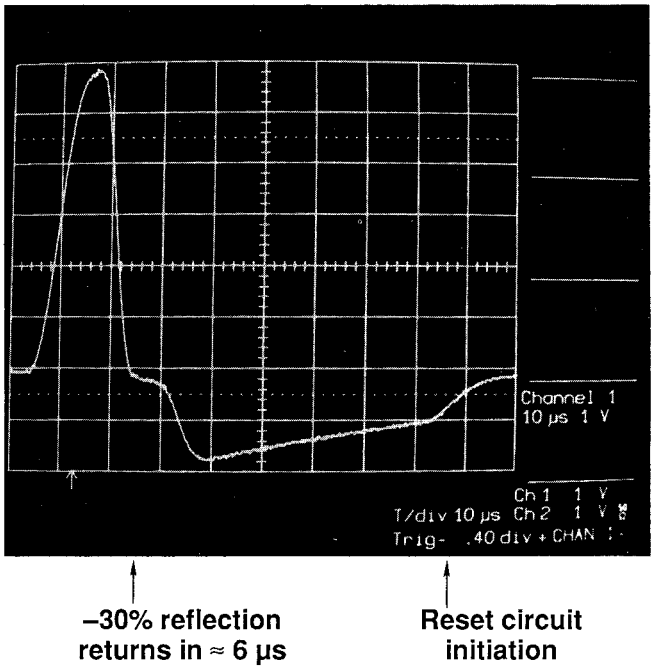


**Figure 6. Voltage at MAG input (15-μs charge, 5-μs discharge, 6-μs delay, and voltage reversal are shown).**

The output of the MAG must arrive at the cell simultaneously with the injected electron beam pulse ($\Delta t < 1$ ns). For the saturable core to saturate with a subnanosecond temporal resolution, it must be reset to the same point (reset circuit dc current bias, not shown), be excited with the same voltage (voltage regulation ≤ 0.04%), and have minimal switch-induced timing jitter (<<1 ns). The goal of this test model is to achieve these results.

**Table 2. Validated operating points for test circuit.**

| Parameter | Symbol | Value |
|---|---|---|
| Average power (each SCR) | $P_{AV}$ | 200 kW (DRC); 80 kW (IES) |
| Voltage (each SCR) | $V_D$ | 600 V (50% derating from 1200 V for safety factor) |
| Average current | $I_{AV}$ | 630 A (DRC); 255 A (IES) |
| Pulse width | $\tau$ | 55 μs (DRC); 15 μs (IES) |
| Recovery time | $t_q$ | <10 μs, 30 V/μs to 180 V, $T_J$ = 100°C |
| Frequency | $f$ | 11 kHz (limited by DRC pulse width) |
| Switch jitter | $j$ | 68 ps |

## Test Results

Operational results from the circuit shown in Fig. 1 have validated the operating points shown in Table 2. Battery power limitations (60 kW and 45 s) have limited long-pulse runs to 6 kHz and 45 s. Calorimetric loss measurements of 0.26 J/pulse on the IES SCR and 0.10 J/pulse on the DRC SCR are the bases for the extrapolation to 80-kW and 200-kW average power.

## Conclusions

Thyristors offer a viable option for use as the switching element in short-pulse, low-jitter magnetic pulse compressors. Virtually any power level can be achieved through the use of series-parallel arrays of devices. Inherent advantages include long lifetime, high reliability, short recovery times, and high-frequency capability.

Feed-forward regulation with a dual resonant circuit can obtain a high degree of voltage regulation. Regulating with the pulse-power circuit in a quiescent state allows the technique to be scaled to the power levels found in high-power accelerators and lasers.

## Acknowledgments

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## References

[1] See M. A. Newton and J. A. Watson, "Timing and Voltage Control for Magnetic Modulators on ETA II," in these conference proceedings.

[2] C. H. Smith, "Permeabilities of Metallic Glasses at High Magnetization Rates," in Proceedings of the Eighteenth Power Modulator Symposium, June 20–22, 1988, p. 336.

[3] S. E. Ball, et al., "Saturable Inductors as High Power Switches," in Proceedings of the Third IEEE Pulsed Power Conference, Albuquerque, N. Mex., June 1–3, 1981, p. 269.